Claims

[c1] A heterojunction bipolar transistor (HBT), comprising:
a collector;
an intrinsic base overlying said collector, said intrinsic base including a layer of a single-crystal semiconductor alloy;
a raised extrinsic base including a first semiconductive layer overlying said intrinsic base and a second semiconductive layer formed on said first semiconductive layer, said first semiconductive layer being etch distinguishable from said second semiconductive layer; and
an emitter overlying said intrinsic base, said emitter disposed in an opening of said first and second semiconductive layers, such that said raised extrinsic base is self-aligned to said emitter.

[c2] The HBT according to claim 1 wherein said emitter is spaced from said raised extrinsic base by a dielectric spacer formed on a sidewall of said opening.

[c3] The HBT according to claim 2 wherein said dielectric spacer includes an oxide spacer contacting sidewalls of said first and said second semiconductive layers and a nitride spacer contacting a sidewall of said oxide spacer.

[c4] The HBT according to claim 2 wherein said dielectric spacer includes a nitride spacer overlying an oxide layer, said nitride spacer contacting sidewalls of said first and said second semiconductive layers.

[c5] The HBT according to claim 1 wherein said first semiconductive layer has a first composition $Si_{x1}Ge_{y1}$, where x1 and y1 represent percentages of silicon and germanium of said first composition, respectively, and said second semiconductive layer has a second composition $Si_{x2}Ge_{y2}$, where x2 and y2 represent percentages of silicon and germanium of said second composition, respectively, said percentages y1 and y2 of germanium being sufficiently different to make said first semiconductive layer etch distinguishable from said second semiconductive layer.

[c6] The HBT according to claim 5 wherein at least one of said percentages y1 and y2 of germanium varies as a function of vertical position over a thickness of said first semiconductive layer or said second semiconductive layer, respectively.

[c7] The HBT according to claim 5 wherein said first semiconductive layer has a first dopant concentration, and said second semiconductive layer has a second dopant

concentration, wherein at least one of said first and second dopant concentrations varies as a function of vertical position over a thickness of said first semiconductive layer or said second semiconductive layer, respectively.

[c8] The HBT according to claim 1 wherein said second semiconductive layer consists essentially of an alloy of silicon and germanium and said first semiconductive layer consists essentially of silicon.

[c9] The HBT according to claim 5 wherein said second semiconductive layer has a substantially greater percentage of germanium than said first semiconductive layer.

[c10] The HBT according to claim 9 wherein said second semiconductive layer has substantially greater thickness than said first semiconductive layer.

[c11] The HBT according to claim 9 wherein said first semiconductive layer has a first dopant concentration, and said second semiconductive layer has a second dopant concentration, wherein said first and said second dopant concentrations are substantially different from each other.

[c12] The HBT according to claim 9 wherein said first and second semiconductive layers include at least portions having a single-crystal structure.

[c13] The HBT according to claim 1 wherein said raised extrinsic base includes a low resistance layer formed above said second semiconductive layer, said low resistance layer including at least one material selected from metals and metal silicides.

[c14] The HBT according to claim 13 wherein said low resistance layer includes a salicide, said salicide being a self-aligned silicide formed by depositing a layer of silicon over said second semiconductive layer, depositing a metal onto said silicon layer, and reacting said metal with said silicon to form said salicide.

[c15] A heterojunction bipolar transistor (HBT), comprising:
a collector;
an intrinsic base overlying said collector, said intrinsic base including first and second layers, said first layer consisting essentially of an alloy of silicon and germanium, said second layer consisting essentially of silicon;
a raised extrinsic base including a first semiconductive layer overlying said intrinsic base, said first semiconductive layer having a first composition according to $Si_{x1}Ge_{y1}$, x1 and y1 being complementary percentages, said raised extrinsic base further including a second semiconductive layer formed on said first semiconductive layer, having a second composition according to $Si_{x2}Ge$

, x2 and y2 being complementary percentages, wherein said percentage y2 is substantially greater than said percentage y1, said second semiconductive layer being etch distinguishable from said first semiconductive layer; and

an emitter overlying said intrinsic base, said emitter disposed in an opening of said first and second semiconductive layers, said emitter spaced from said raised extrinsic base by at least one dielectric spacer formed on a sidewall of said opening.

[c16] A method of making a heterojunction bipolar transistor, comprising:

forming a collector;

forming an intrinsic base overlying said collector, said intrinsic base including a layer consisting essentially of an alloy of silicon and germanium;

forming a raised extrinsic base by steps including

forming a first semiconductive layer over said intrinsic base;

forming a second semiconductive layer contacting said first semiconductive layer; and

vertically etching an opening in said second semiconductive layer, stopping on said first semiconductive layer;

extending said opening downwardly through said first semiconductive layer to expose said intrinsic base; and

forming an emitter contacting said intrinsic base in said extended opening, such that said raised extrinsic base is self-aligned to said emitter.

[c17] The method according to claim 16 further comprising forming a dielectric spacer on a sidewall of said opening prior to forming said emitter such that said emitter is spaced from said raised extrinsic base by said dielectric spacer.

[c18] The method according to claim 17 wherein said dielectric spacer includes a nitride spacer overlying an oxide layer, said nitride spacer formed on sidewalls of said first and said second semiconductive layers.

[c19] The method according to claim 16 wherein said first semiconductive layer has a first composition $Si_{x1}Ge_{y1}$, where x1 and y1 are percentages of silicon and germanium in said first composition, and said second semiconductive layer has a second composition $Si_{x2}Ge_{y2}$, where x2 and y2 are percentages of silicon and germanium in said second composition, wherein said percentages y1 and y2 are sufficiently different such that said first semiconductive layer is etch distinguishable from said second semiconductive layer.

[c20] The method according to claim 19 wherein said percent-

age y2
is substantially higher than said percentage y1.

[c21] The method according to claim 19 wherein said second semiconductive layer has substantially greater thickness than said first semiconductive layer.

[c22] The method according to claim 19 wherein said first semiconductive layer has a first dopant concentration, and said second semiconductive layer has a second dopant concentration, wherein said first and said second dopant concentrations are substantially different from each other.

[c23] The method according to claim 19 wherein at least one of said percentages y1 and y2 of germanium varies as a function of vertical position over a thickness of said first semiconductive layer or said second semiconductive layer, respectively.

[c24] The method according to claim 19 wherein said first semiconductive layer has a first dopant concentration, and said second semiconductive layer has a second dopant concentration, wherein at least one of said first and second dopant concentrations varies as a function of vertical position over a thickness of said first semiconductive layer or said second semiconductive layer, re-

spectively.

[c25] The method according to claim 14 wherein said first and second semiconductive layers are formed by blanket epitaxial growth over said intrinsic base.

[c26] The method according to claim 16 wherein said opening is extended downwardly by forming a dielectric spacer on a sidewall of said opening and wet etching said first semiconductive layer from a bottom of said opening.

[c27] The method according to claim 16 wherein said opening is extended downwardly by forming a dielectric spacer on a sidewall of said opening and oxidizing said first layer of said intrinsic base from within said opening.

[c28] The method according to claim 27 wherein said step of forming said raised extrinsic base further includes forming a low resistance layer above said second semiconductive layer, said low resistance layer including at least one material selected from metals and metal silicides.

[c29] The method according to claim 28 wherein said low resistance layer includes a salicide, said salicide being a self-aligned silicide formed by depositing a layer of silicon over said second semiconductive layer, depositing a metal onto said silicon layer, and reacting said metal with said silicon to form said salicide.